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KIT33907AEEVB and KIT33908AEEVB Evaluation Board

MC33907 and MC33908 Safe System Basis Chips

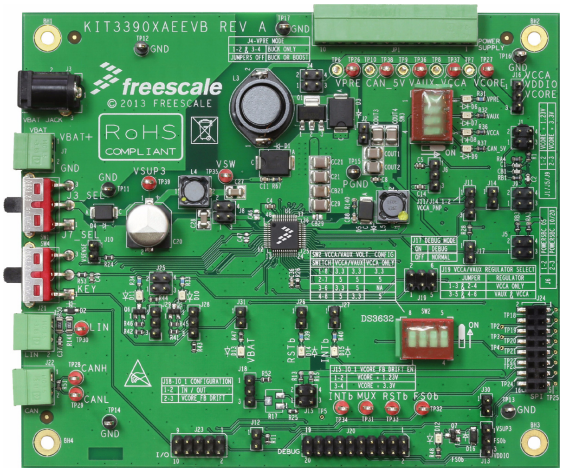

Figure 1. KIT33907AEEVB or KIT33908AEEVB Evaluation Board

Contents

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1 Kit Contents/Packing List

- Assembled and tested evaluation board/module in anti-static bag.
- Warranty card

2 Jump Start

- Go to www.freescale.com/analogtools
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3 Terms

Part Number or Parameter	Definitions
SPIGen	Software utility (installed on a PC) that provides communication functions between the PC and a Freescale evaluation board.
WD	Watchdog
FCCU	Fault Collection and Control Unit
SMPS	Switching mode power supply
LDO	Low-dropout regulator
EVB	Evaluation Board
V_{PRE}	Pre-regulator voltage
V_{AUX}	Auxiliary power supply
V_{CCA}	Power supply for ADC
CAN_5V	5.0 V CAN voltage
IO	Input/output
FS0B	Fail-safe output no. 0
RSTB	Reset
INTB	Interrupt

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5 Introduction

KIT33907AEEVB and KIT33908AEEVB evaluation boards demonstrate the functionality of the SMARTMOS MC33907 and MC33908 power system basis chips, respectively. These ICs are equipped with an Intelligent Power Management System including safety features targeting the latest ISO26262 automotive functional safety standard. The evaluation board is a standalone board that can be used either with a compatible microcontroller or with a PC. In the latter case, it is necessary to use an KITUSBSPIDGLEVME accessory interface board. See section “Required Equipment”.

6 Evaluation Board Features

This evaluation board comes mounted with either an MC33907 or an MC33908 IC. The main features of the board are as follows:

- V_{BAT} power supply either through power jack (2.0 mm) or phoenix connector
- V_{CORE} configuration:1.23 V or 3.3 V
- V_{CCA} configuration:
  - 5.0 V/3.3 V
  - Internal transistor or external PNP
- V_{AUX} configuration:
  - 3.3 V or 5.0 V
  - Enabled or disabled at startup
- Ignition key switch
- LIN bus
- CAN bus
- IO connector (IO_0 to IO_5)
- Debug connector (SPI bus, CAN digital, LIN digital, RSTB, FS0B, INTB, Debug, MUX_OUT)
- Signalling LED to give state of signals or regulators

7 MC33907 and MC33908 Device Features

The MC33907 and the MC33908 are multi-output ICs, with power supply and HSCAN transceiver. These devices have been designed specifically with the automotive market in mind. The MC33907 is designed to support up 800 mA on V_{CORE}, while MC33908 will support up to 1.5 A on V_{CORE}. All other features are the same. Both devices support following functions:

- Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost or standard buck
- Switching mode power supply (SMPS) dedicated to MCU core supply: 1.2 V or 3.3 V, delivering up to 1.5 A for the MC33908 and up to 800 mA for the MC33907
- Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (VCCA): 5.0 V or 3.3 V
- Linear voltage regulator dedicated to auxiliary functions or to a sensor supply (VCCA tracker or independent 5.0 V/3.3 V)
- Multiple wake-up sources in Low-power mode: CAN and/or IOs
- Battery voltage sensing and multiplexer output terminal (various signal monitoring)
- Enhanced safety block associated with fail-safe outputs
- Six configurable I/Os
- ISO11898 high speed CAN interface compatibility for baud rates of 40 kB/s to 1.0 MB/s
- High EMC immunity and ESD robustness

8 Required Equipment

Minimum equipment required:

- Power supply: 2.7 V to 40 V with 3.0 A capability

Note: When not connected to an MCU, the KITUSBSPIDGLVME can be used for register setting. In this case, the SPIgen dongle and USB cable are required. For more information, see the “SPIgen 7 User Guide”.

9 Evaluation Board Hardware Description

The evaluation board comes with either a Freescale MC33907 or MC33908 IC mounted on it. Below is a board-level logic diagram.

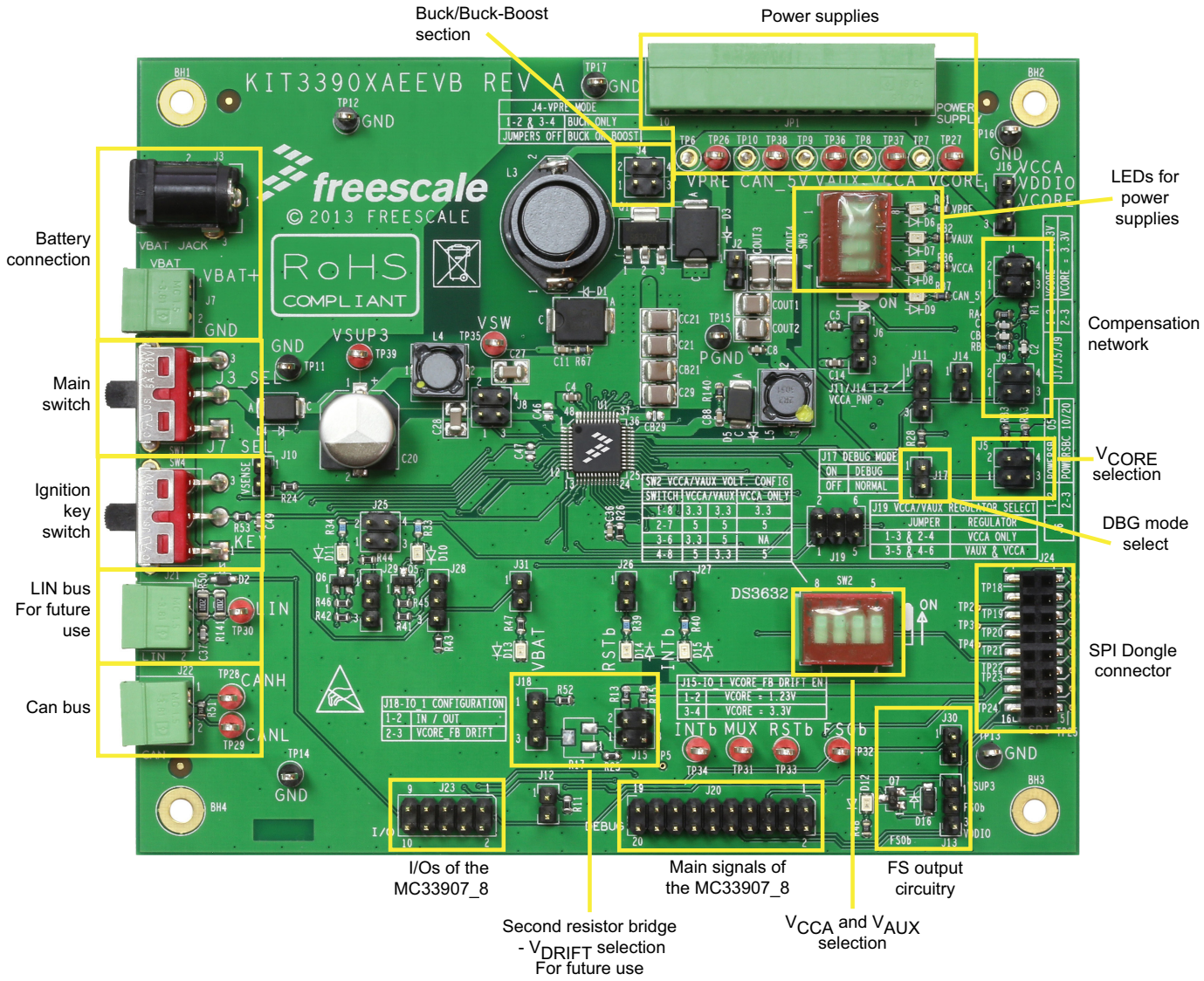


Figure 2. Block Diagram for KIT33907AEEVB and KIT33908AEEVB

9.1 Evaluation Board Configuration

Figure 3 shows a configuration example for the EVB, which enables:

- V_{CORE} 3.3 V
- Compensation network for MPC5643L
- V_{CCA} & V_{AUX} = 5.0 V
- V_{CCA} with external PNP
- Debug mode
- V_{PRE} in Buck mode
- V_{DDIO} tied to V_{CCA}
- Various signalling LEDs enabled
- IO1 configured as IN/OUT

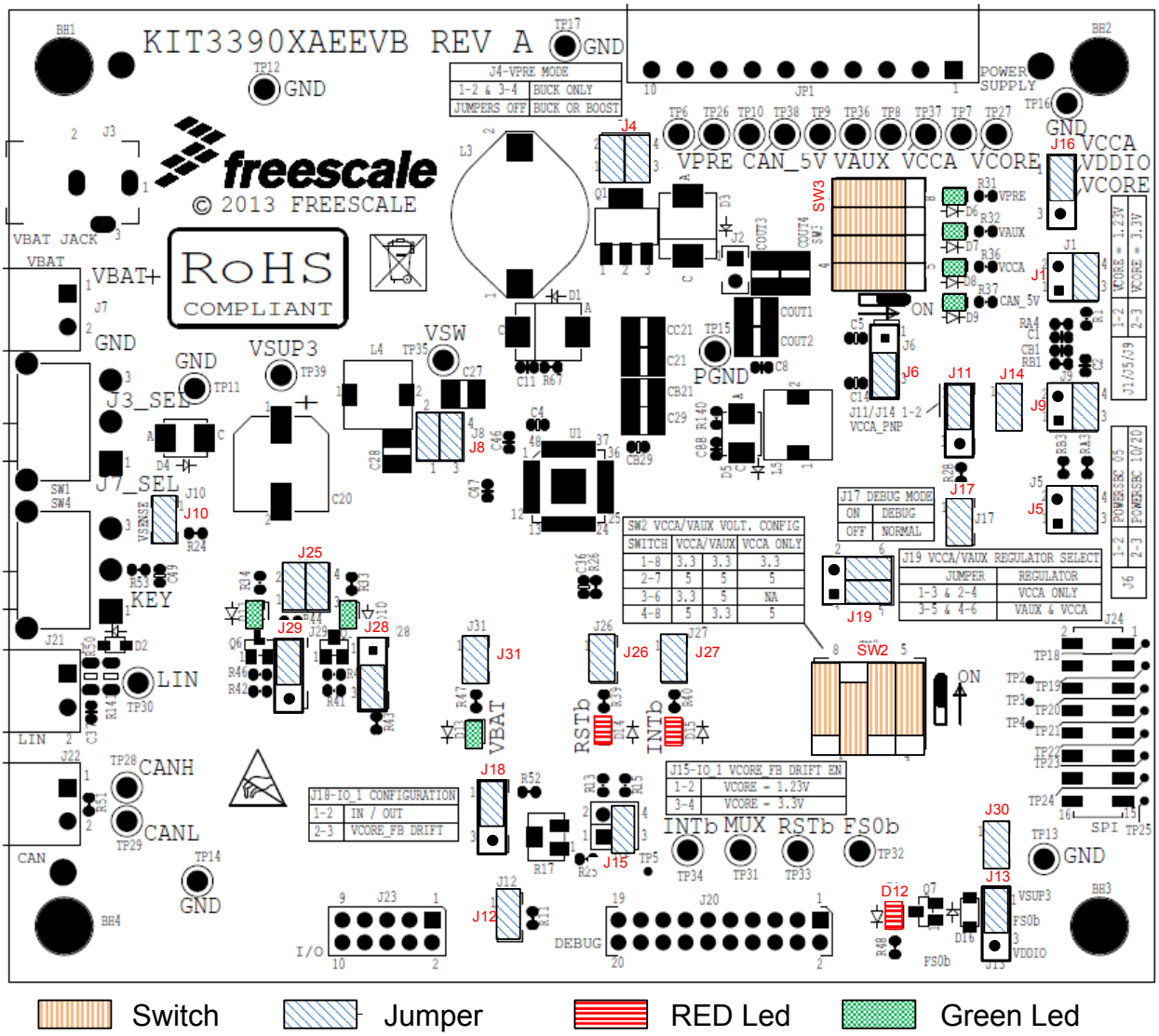


Figure 3. Default Board Configuration

9.2 LED Definitions

The following table lists the LEDs used as visual output devices on the evaluation board:

Table 1. LEDs

Schematic Label	Name	Description
D6	V_{PRE}	Indicator of pre-regulator voltage
D7	V_{AUX}	Indicator of auxiliary power supply
D8	V_{CCA}	Indicator of ADC power supply
D9	CAN_5V	Indicator of 5.0 V CAN voltage
D10	IO_5	Indicator of IO_5 state
D11	IO_4	Indicator of IO_4 state
D12	FS0B	Indicator for Fail-safe output no. 0
D13	Vbat_P	Indicator of battery voltage after protection diode
D14	RSTB	Indicator of a reset
D15	INTB	Indicator of an interrupt

9.3 Test Point Definitions

The following test-point jumpers provide access to signals on the MC33907 or MC33908 IC:

Table 2. Test Points

Schematic Label	Signal Name	Description
TP2	J24.3	-
TP3	J24.5	-
TP4	J24.7	-
TP5	J20.16	-
TP6	PGND	Power ground
TP7	PGND	Power ground
TP8	GND	Ground
TP9	GND	Ground
TP10	GND	Ground
TP11	GND	Ground
TP12	GND	Ground
TP13	GND	Ground
TP14	GND	Ground
TP15	GND	Ground
TP16	GND	Ground
TP17	GND	Ground
TP18	J24.2	-

Table 2. Test Points (continued)

Schematic Label	Signal Name	Description
TP19	J24.4	-
TP20	J24.6	-
TP21	J24.8	-
TP22	J24.10	-
TP23	J24.12	-
TP24	J24.14	-
TP25	J24.16	-
TP26	V_{PRE}	Pre-regulator voltage
TP27	V_{CORE}	Core voltage for the MCU
TP28	CANH	-
TP29	CANL	-
TP30	LIN	LIN bus
TP31	MUX_OUT	Output from the analog multiplexer
TP32	FS0B	Fail-safe output
TP33	RSTB	Reset signal
TP34	INTB	Interrupt output
TP35	V_{SW}	V_{PRE} Switching voltage
TP36	V_{AUX}	Auxiliary power supply
TP37	V_{CCA}	ADC power supply
TP38	CAN_5V	CAN power supply
TP39	V_{SUP3}	Supply voltage

9.4 Connector and Jumper Definitions

Table 3. Main Power Supply Connector

JP1 Pin Number	Name of Power Rail	Description
1	V_{CORE}	Core voltage for the MCU
2	PGND	Power ground
3	V_{CCA}	ADC power supply
4	GND	Ground
5	V_{AUX}	Auxiliary power supply
6	GND	Ground
7	CAN_5V	CAN power supply
8	GND	Ground
9	V_{PRE}	Pre-regulator voltage
10	PGND	Power ground

Table 4. Jumpers J1 through J31 (Including Connectors)

Schematic Label	Pin Number	Pin Name	Jumper/Pin Function
J1	Compensation network for FB_core – part 1		
	1-2		V_{CORE} = 1.23 V
	3-4		V_{CORE} = 3.3 V
J2	C_OUT – selection of the output capacitance for V_{CORE}. If connected, the output capacitance is 40 µF, 20 µF otherwise.		
	No jumper		C_{OUT} = 20 µF
	1-2		C_{OUT} = 40 µF
J3	Power supply DC 12 V		
J4	Buck-boost/standard buck mode configuration		
	1-2		Buck-boost configuration
	3-4		
	No jumper		Buck only configuration
J5	V_{CORE} selection		
	1-2		V_{CORE} = 1.23 V
	3-4		V_{CORE} = 3.3 V
J6	Configuration for Boots_core pin		
	1-2		Boots_core pin connected to GND – used for devices with linear voltage regulator on V_{CORE}
	2-3		Boots_core pin connected to SW_core – used for devices with switching mode power Supply on V_{CORE}

Table 4. Jumpers J1 through J31 (Including Connectors) (continued)

Schematic Label	Pin Number	Pin Name	Jumper/Pin Function
J7	Power supply (max. voltage = 40 V) This connector should be used to supply evaluation board from protected voltage source.		
	1	VBAT	Positive supply
	2	GND	Ground
J8	Power supply for evaluation board Allows disconnecting of all three supply pins for current measurements. Normally (no measurement), jumpers should be connected.		
	1-2		Enables power supply (V_{BAT_P}) for VSUP3 pin of the MC33907 (or MC33908)
	3-4		Enables power supply (V_{SUP}) for VSUP1 and VSUP2 pins of the MC33907 (or MC33908)
J9	Compensation network for FB_core – part 2		
	1-2		V_{CORE} = 1.23 V
	3-4		V_{CORE} = 3.3 V
J10	Vsns_EN – connects battery voltage before filter to the V_{SENSE}		
J11	External transistor for V_{CCA}		
	1-2		Emitter of Q2 connected to VCCA_E
	2-3		External transistor Q2 is not used
J12	IO_0_PD – pulls down IO_0		
J13	FS0B pull-up connection		
	1-2		FS0B pull-up is supplied from V_{SUP3}
	2-3		FS0B pull-up is supplied from V_{DDIO}
J14	Connects base of the transistor Q2 to the VCCA_B pin		
J15	External resistor bridge monitoring for future use Used in conjunction with J18. This resistor bridge has to be in the same configuration as the J5. The voltage on this voltage divider has to be adjusted to the same level as for the first bridge using potentiometer R17.		
	1-2		V_{CORE} =1.23 V
	3-4		V_{CORE} = 3.3 V
J16	V_{DDIO} tracking		
	1-2		V_{DDIO} tracks V_{CCA}
	2-3		V_{DDIO} tracks V_{CORE}
J17	DBG_EN - enables debug mode		
	No jumper		Normal mode
	1-2		Debug mode
J18	DRIFT_MONIT – External resistor bridge monitoring for future use		
	1-2		Second resistor bridge on IO_1 is disabled
	2-3		Reserved for future use
J19	V_{CCA}/V_{AUX} regulator selection		
	1-3 and 2-4		V_{AUX} is disabled
	3-5 and 4-6		V_{AUX} is enabled

Table 4. Jumpers J1 through J31 (Including Connectors) (continued)

Schematic Label	Pin Number	Pin Name	Jumper/Pin Function
J20	Additional Inputs/Output		
	1	FS0B	Fail-safe output
	2	VDDIO	V_{DDIO} voltage
	3	MISO	SPI – Master Input Slave Output
	4	RSTB	Reset pin – connect to the reset line of the MCU
	5	MOSI	SPI – Master Output Slave Input
	6	GND	Ground
	7	SCLK	SPI – clock
	8	GND	Ground
	9	NCS	SPI – Chip Select
	10	GND	Ground
	11	MUX_OUT	Output from the multiplexer – connect to the MCU's ADC
	12	INTB	Interrupt pin – connect to the MCU IO with an interrupt capability
	13	RXD_L	LIN receive pin – connect to the MCU. For future use
	14	TXD_L	LIN transmit pin – connect to the MCU. For future use
	15	GND	Ground
	16	TP5	-
	17	RXD	CAN receive pin – connect to the MCU
	18	TXD	CAN transmit pin – connect to the MCU
	19	DBG	Debug pin
	20	GND	Ground
J21	LIN connector		
	1	LIN	LIN after transceiver (NOT the MCU side). For future use
	2	GND	Ground
J22	CAN connector		
	1	CANH	CANH signal after transceiver (NOT the MCU side)
	2	CANL	CANL signal after transceiver (NOT the MCU side)

Table 4. Jumpers J1 through J31 (Including Connectors) (continued)

Schematic Label	Pin Number	Pin Name	Jumper/Pin Function
J23	General Inputs/Outputs		
	pin1	IO_1	-
	pin2	IO_0	-
	pin3	IO_3	-
	pin4	IO_2	-
	pin5	IO_5	-
	pin6	IO_4	-
	pin7	VDDIO	-
	pin8	NC	-
	pin9	VBAT	-
	pin10	GND	-
J24	SPI/USB dongle or MCU connection SPI/USB dongle should be directly connected to this port		
	pin1	GND	Ground
	pin2	TP18	-
	pin3	TP2	-
	pin4	TP19	-
	pin5	TP3	-
	pin6	TP20	-
	pin7	TP4	-
	pin8	TP21	-
	pin9	SCLK	SPI – clock
	pin10	TP22	Not connected
	pin11	MOSI	SPI – Master Output Slave Input
	pin12	TP23	-
	pin13	MISO	SPI – Master Input Slave Output
	pin14	TP24	-
	pin15	NCS	SPI – Chip Select
	pin16	TP25	-
J25	Power supply for LEDs on IO_4 and IO_5 (D11, D10)		
	1-2		Enables power supply for IO_4 (D11)
	3-4		Enables power supply for IO_5 (D10)
J26	RSTB_LED_EN – enables LED D14 for RSTB output		
J27	INTB_LED_EN – enables LED D15 for INTB output		
J28	IO5_OUT – IO_5 output configuration		
	1-2		IO_5 connected to the LED D10 via transistor Q5
	2-3		IO_5 pulled down
J29	IO4_OUT – IO_4 output configuration		
	1-2		IO_4 pulled down
	2-3		IO_4 connected to the LED D11 via transistor Q6

Table 4. Jumpers J1 through J31 (Including Connectors) (continued)

Schematic Label	Pin Number	Pin Name	Jumper/Pin Function
J30	Enable LED D12 for Fail-safe 0.		
J31	Enables LED D13 as indicator of power supply		

9.4.1 Compensation Network

Voltage regulator needs a feedback from the V_{CORE} voltage to be able to adjust (control) output voltage. For this reason two bridges are implemented in the external MC33907 or MC33908 circuitry. Static feedback (steady-state) voltage is defined by a simple resistor bridge (given by RA3/RB3 and RA4). Dynamic behavior of the regulator is controlled by another bridge that is an RC divider (defined by RBx, CBx, R1, C1, R2, C2). Compensation network is shown in the Figure 4. Steady-state voltage can be either 1.23 or 3.3 V. To tune the dynamic performance, the board is equipped by two different bridges (possible combinations of the jumpers J1 and J9 are shown in Table 5). The combinations shown in Table 5 are chosen to provide an optimal performance for the given output voltage. The real dynamic performance can differ for different applications and can be tuned by changing the compensation network and by adding output capacitors (J2).

Table 5. Compensation Network and V_{CORE} Settings

V_{CORE} (V)	Jumper Settings		
	Static Behavior	Dynamic Behavior	
	J5	J1	J9
1.23	3-4	3-4	3-4
3.3	1-2	1-2	1-2

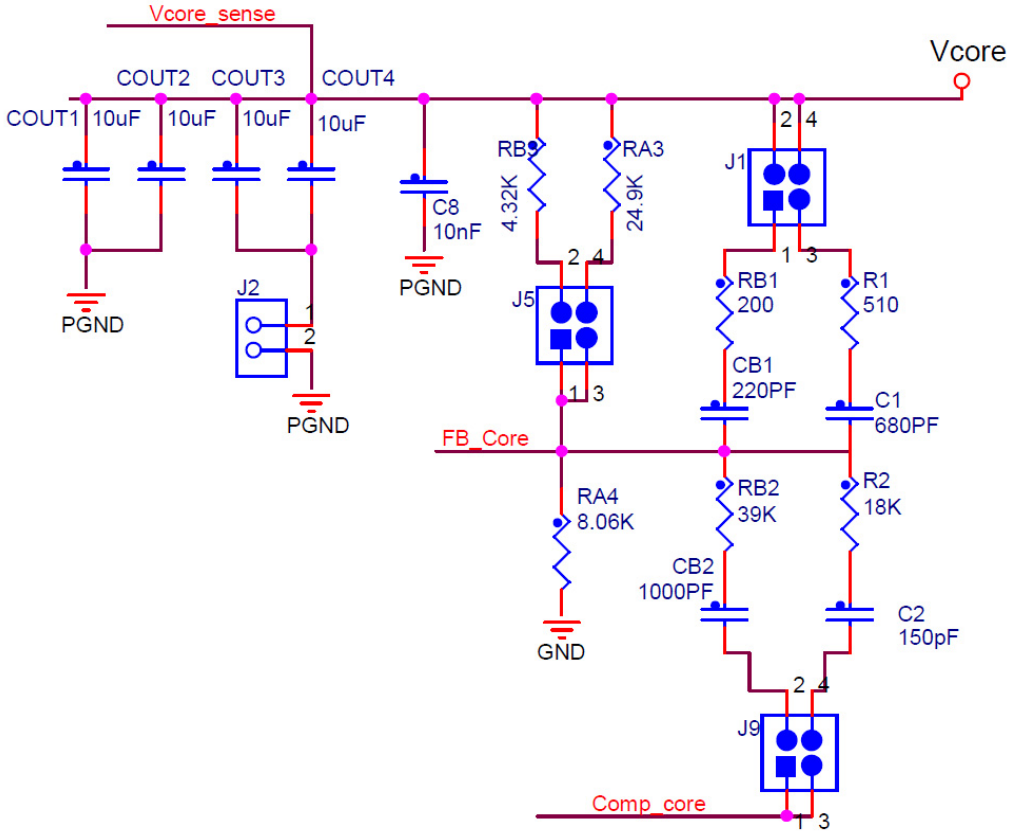


Figure 4. Compensation Network and V_{CORE} Setup Schematic

9.4.2 Second Resistor Bridge - V_{DRIFT} Monitoring (for future use)

To increase safety level of an application, a second resistor bridge has been added for future use. This bridge generates the same voltage as the bridge connected to FB_core pin. If difference between voltages is greater than V_{DRIFT}, then the FS state machine is impacted.

Table 6. V_{DRIFT} Monitoring Settings

V_{CORE} (V)	Hardware Settings	
	J15	J18
1.23	1+2	3+4
3.3	3+4	1+2

To use this functionality, few settings have to be done in the hardware as well as in the software configuration. For the hardware part, the second resistor bridge has to be configured by jumper J18, as shown in the Figure 5, and adjusted by the potentiometer R17 to set the same voltage as on the first bridge. Software sets registers INIT_Vreg1 (bit Vcore_FB to 1) and register INIT_FSSM1 (bit IO_1_FS to 1). This functionality is not supported by the MC33907_8AE version and is intended for future use.

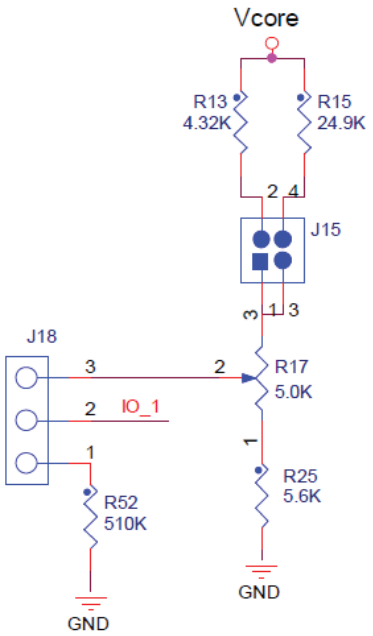


Figure 5. Second Resistor Bridge

9.5 Switch Definitions

Table 7. Switches

Switch No.	Position	Function	Description
SW1	Power supply select		
	1-2	Supply from J7 selected	
	2-3	Power jack on J3 selected	
SW2	V_{CCA}/V_{AUX} switch. Only one choice is possible at the same time		
	1	3.3 V / 3.3 V	
	2	5.0 V / 5.0 V	
	3	3.3 V / 5.0 V	This setting is not allowed if V_{AUX} is not used - option V_{CCA} only (selected by J19)
	4	5.0 V / 3.3 V	
SW3	LEDs - indicators for Power supplies		
	1	V_{PRE}	Enables LED indicator for pre-regulator
	2	V_{AUX}	Enables LED indicator for auxiliary power supply
	3	V_{CCA}	Enables LED indicator for V_{CCA} regulator
	4	CAN_5 V	Enables LED indicator for CAN regulator
SW4	Ignition switch		
	1-2	IO_0 connected to V_{BAT} (ignition key active)	
	2-3	No voltage on the IO_0	

10 Accessory Interface Board

The KIT33907AEEVB or KIT33908AEEVB is generally used with the KITUSBSPIDGLEVME interface dongle (shown below), which provides a bidirectional SPI/USB conversion. This small board makes use of the USB, SPI, and parallel ports built into Freescale's MC68HC908JW32 microcontroller. The main function provided by this dongle is to allow Freescale evaluation kits that have a parallel port to communicate via a USB port to a PC. For more information regarding KITUSBSPIDGLEVME interface dongle, go to http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KITUSBSPIDGLEVME.

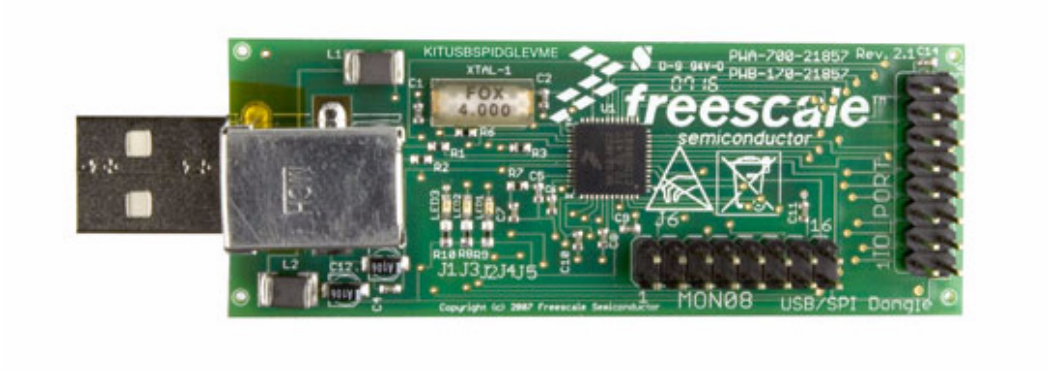


Figure 6. KITUSBSPIDGLEVME Interface Dongle

For information on setting up the dongle with the evaluation board, see section "Connecting the KITUSBSPIDGLEVME Interface Dongle".

11 Connecting the KITUSBSPIDGLEVME Interface Dongle

A typical connection of KITUSBSPIDGLEVME Interface Dongle (section “Accessory Interface Board”) to the KIT33907AEEVB or KIT33908AEEVB evaluation board is done through connector J24 (see Figure 7). In this configuration, it is recommended to use the evaluation board in a debug mode (J17 configured as Debug). In this mode there is no time-out used for the INIT phase, so the initialization commands can be sent anytime. WD refresh is also not mandatory in the debug mode. This means that no action is taken if WD refresh fails (WD window expires, WD refreshed during closed window, wrong WD answer).

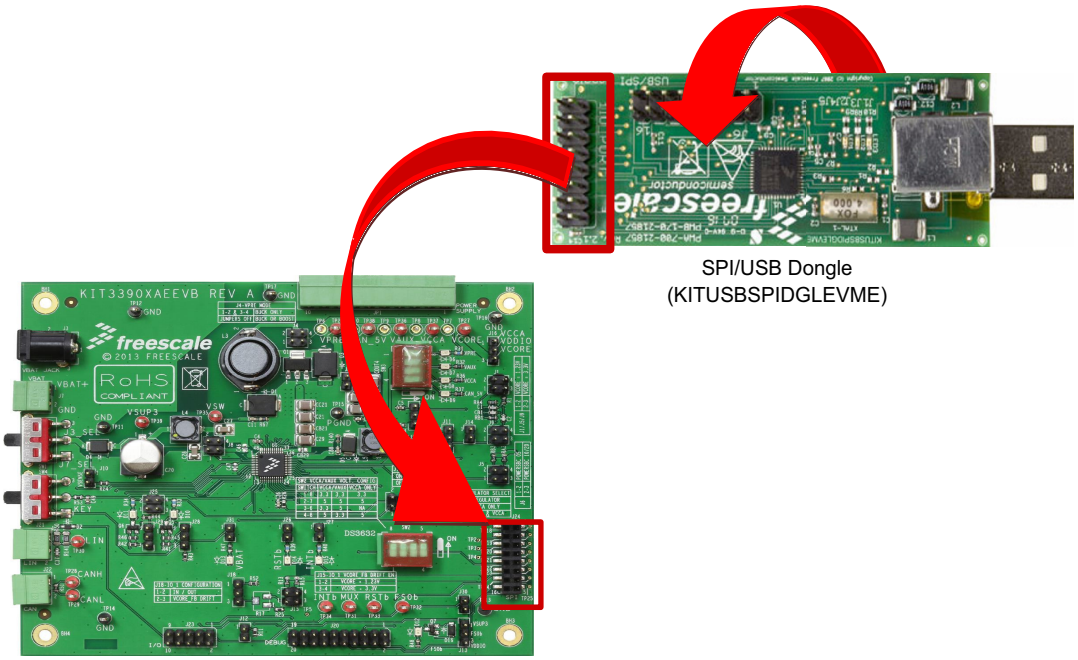


Figure 7. Installation of KITUSBSPIDGLEVME on Evaluation Board

11.1 Evaluation Board Setup

The figure below shows the setup required to use KIT33907AEEVB and KIT33908AEEVB.

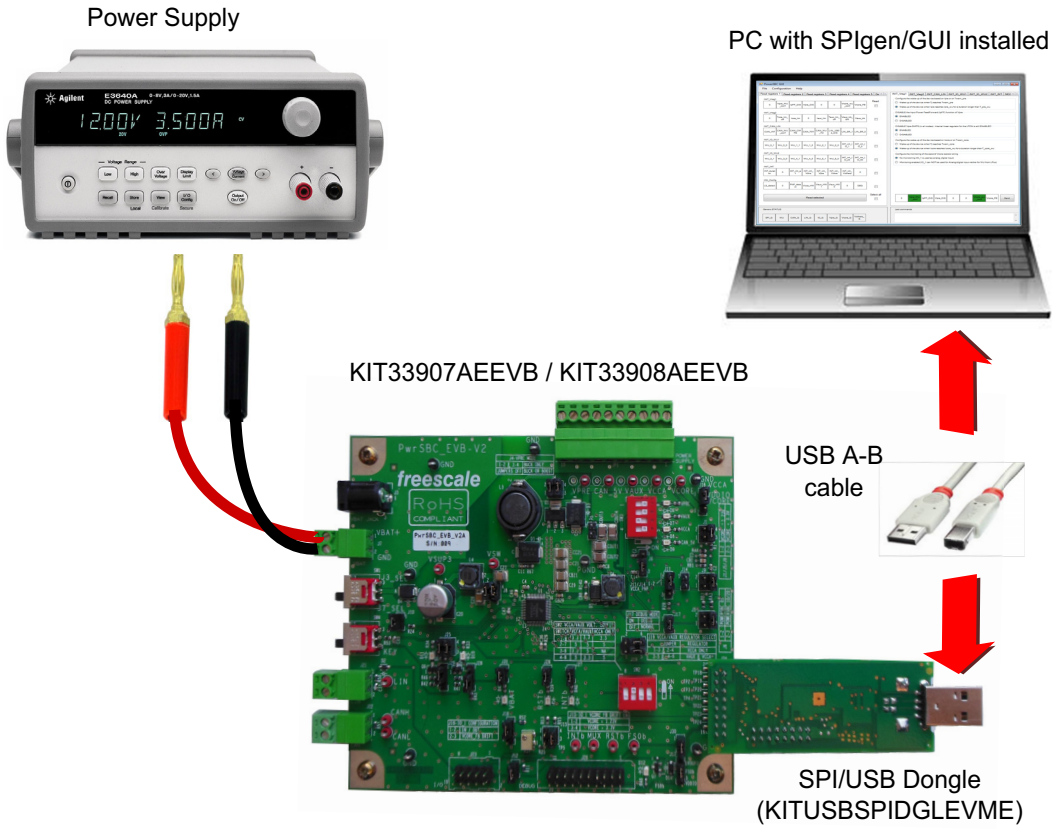


Figure 8. Evaluation Board Setup

11.2 Setting Up and Using the Hardware

11.2.1 Step-by-Step Instructions

In order to perform the demonstration examples, first set up the evaluation board hardware and software as follows:

1. Ready the computer, install SPIgen.
2. Connect SPIgen on J24.
3. Connect SPIgen USB cable to the PC.
4. Set the EVB jumpers and switches as needed. Refer to Figure 3 for an example.
5. Select Debug or Normal mode with J17 (1).
6. Attach loads to JP1 as needed.
7. Attach DC power supply on J3 or J7 (maximum voltage: 40 V).
8. Switch SW1 to supply the board.

9. If SW2 switches are ON and V_{BAT} is set correctly, then V_{PRE}, V_{CCA}, V_{AUX}, CAN_5 V LEDs should turn ON. V_{BAT} value is dependent on V_{PRE} configuration. In Buck mode, it must be 8.2 V min. FS0B LED should turn ON (J13 / J30 must be plugged).
10. Launch SPIgen.
11. Open the SPIgen configuration file.
12. In Debug mode, use the SPIgen batch RST_counter_to_0.spi to reset the error counter. FS0B should turn off (LED D12 turned off).

Note: At this stage, EVB is powered and SPIgen is working. When Normal mode is selected with J17, valid watchdog must be sent, otherwise the device goes into deep Fail-safe.

12 Initialization and Configuration Mode

12.1 INIT Phase

INIT registers are set after POR (power-on reset) condition with their default values. This default configuration is compatible with the default evaluation board settings excluding one register - INIT FSSM2. Bit IO_23_FS in this register is set by default, which means that the fail-safe outputs (FCCU_x of the MPC5643L or similar device) have to be connected to the IOs 2 and 3 of the MC33907 or MC33908. If MPC5643L (or similar device) is not used, the bit IO_23_FS has to be cleared during INIT phase (setting shown in Table 8). INIT phase of the main part is finished after writing to the INIT_INT register. This command closes access to the INIT registers and device goes in Normal mode. This sequence (INIT_FSSM2, INIT_INT) has to be done in the same manner in Debug and also in Standard mode. The only difference is in the time-out constraints used for the Standard mode. In the Standard mode, INIT commands have to be sent before the 256 ms timer (starting from the RST pin release) expires.

Table 8. INIT FSSM2 Setting

	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	**1**	**1**	**0**	**0**	**1**	**0**	**1**	**P**	**RSTB_ err_FS**	**IO_23_ FS**	**PS**	**F_FS1**	**Secure _3**	**Secure _2**	**Secure _1**	**Secure _0**
	bit15	bit14	bit13	bit12	bit11	bit10	bit9	bit8	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
MOSI	**1**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	**1**	**1**	**0**	**0**	**0**

12.2 Normal Operation

During normal operation (after INIT phase), in both modes it is possible to send a WD refresh command. In the Debug mode, no action is performed on a bad WD answer. In Normal mode, the KITUSBSPIDGLEVMESPI interface dongle is not able to guarantee WD refresh period (Windows XP, 7 are not real-time operating systems); nevertheless, WD refresh was successfully tested in Standard mode using WD window duration 512 ms (reconfigured in the INIT phase).

12.3 Debug Mode

The KIT33907AEEVB or KIT33908AEEVB is mainly intended to be used in Debug mode. Use in normal mode requires an MCU to be able to manage the watchdog. To use the part in Normal mode, it is required to send a good watchdog answer at startup, in the 256 ms windows after reset release, then to update the watchdog at the right time. With KIT33907AEEVB or KIT33908AEEVB attached to the KITUSBSPIDGLEVME, this can be done only manually, which is not really feasible.

13 Graphical User Interface

There are two possible interfaces to configure registers:

- SPI generator (SPIgen) allows easy and simple drive, setting registers individually or sending batch of commands.
- MC33907_8 GUI provides friendly access to registers with a visual environment.

13.1 SPI Gen

The latest version of SPIGen is designed to run on any Windows 8, Windows 7, Vista or XP-based operating system. To install the software, go to www.freescale.com/analogtools and select your kit. Click on that link to open the corresponding Tool Summary Page. Look for “Jump Start Your Design”. Download to your computer desktop the SPIGen software as well as the associated configuration file.

Run the install program from the desktop. The Installation Wizard will guide you through the rest of the process.

To use SPIGen, go to the Windows Start menu, then Programs, then SPIGen, and click on the SPIGen icon. The SPIGen Graphic User Interface (GUI) will appear. Go to the file menu in the upper left hand corner of the GUI, and select “Open”. In the file selection window that appears, set the “Files of type:” drop-down menu to “SPIGen Files (*.spi)”. (As an exceptional case, the file name may have a .txt extension, in which case you should set the menu to “All Files (*.*)”.) Next, browse for the configuration file you saved on your desktop earlier and select it. Click “Open”, and SPIGen creates a specially configured SPI command generator for your evaluation board.

In order to fill specific need, it is also possible to edit registers with another value and to save it for further use, either as standalone or inside a batch.

Figure 9 shows a batch called “RST_counter_to_0”, as an example.

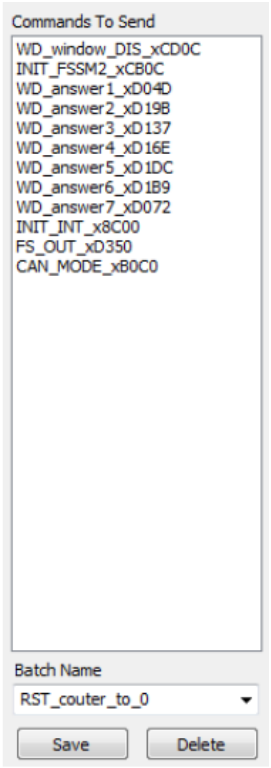


Figure 9. RST_counter_to_0 Batch

At startup or when resuming from LPOFF mode the reset error counter starts at level 1 and FS0B is asserted low. To remove activation of FS0B, the RST error counter must go back to value “0” (seven consecutive good watchdog refresh decreases the reset error counter down to 0) and a right command is sent to FS_OUT register. This can be demonstrated with this batch running in debug mode.

The batch shown in Figure 9 executes the following action:

- WD_Window_DIS_xCD0C:
  - Disables normal watchdog
- INIT_FSSM2_xCB0C:
  - IO_23_FS bits configured in “NOT SAFETY” mode
- WD_answer1 to WD_answer7:
  - If the part is in debug mode, this sends the right first watchdog answer and allows the reset counter to change to 0
- FS_OUT_xD327:
  - Disables FS0B pin, coming back to high level (D12 turned off)
- INIT_INT_x8C00:
  - Closes the init phase of the main state machine
- CAN_MODE_B0C0:
  - Enables CAN transceiver

13.2 Working with KIT33907_8 GUI

The Graphical User Interface allows the user to program all SPI features by using a friendly interface as well as modifying the register table manually for advance users. Refer to KTMPC5643DBEMOUG for a complete description of the GUI.

1. To launch the MC33907_8 GUI application, select the application icon from the Freescale folder in the Start menu as it is shown in the figure below.

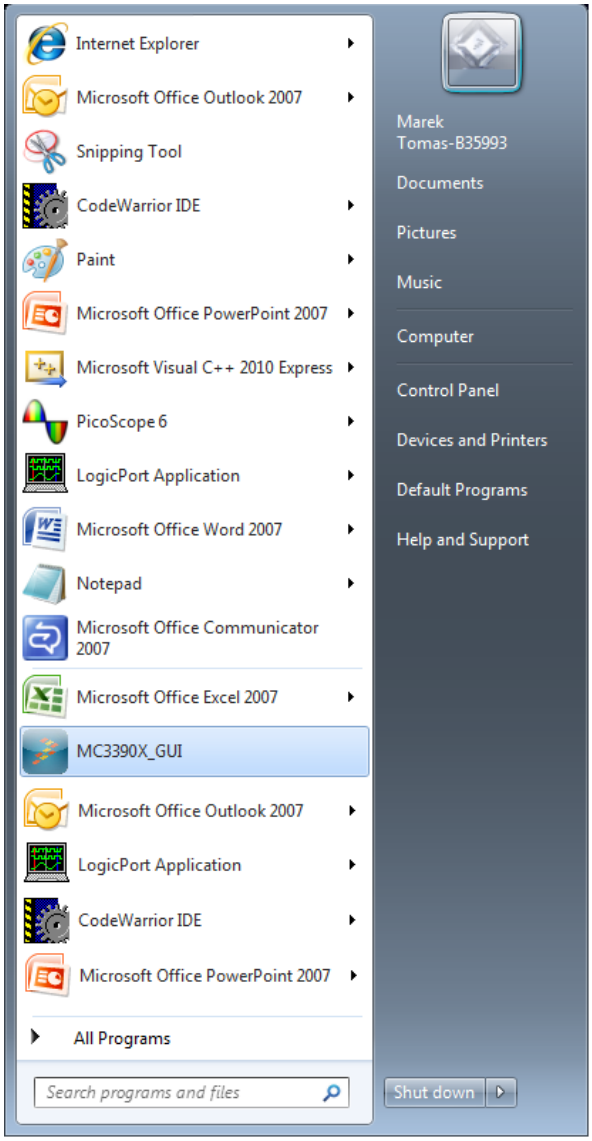


Figure 10. Launching MC33907_8 GUI application

2. Figure 11 shows the status of several registers at startup. In this example, register INIT_FSSM2 has bit IO_23_FS configured as **Safety Critical**.

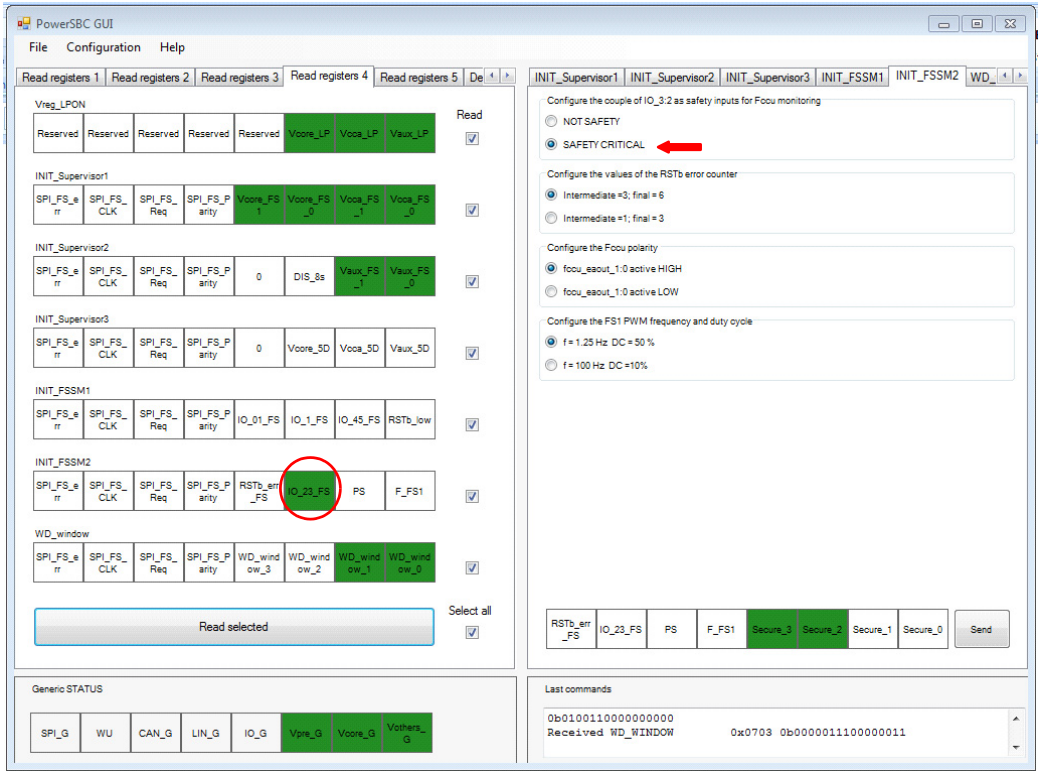


Figure 11. MC33907_8 GUI Main Screen

3. In the right side of the GUI, select **Not Safety** and send command as shown in Figure 12.

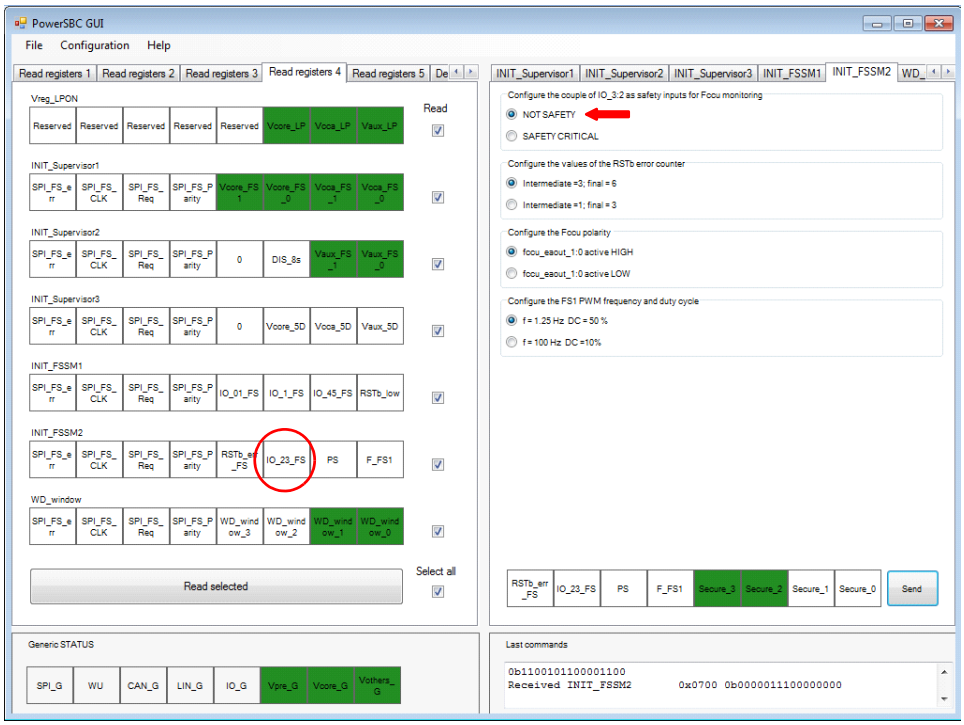


Figure 12. MC33907_8 GUI Register

14 Schematic

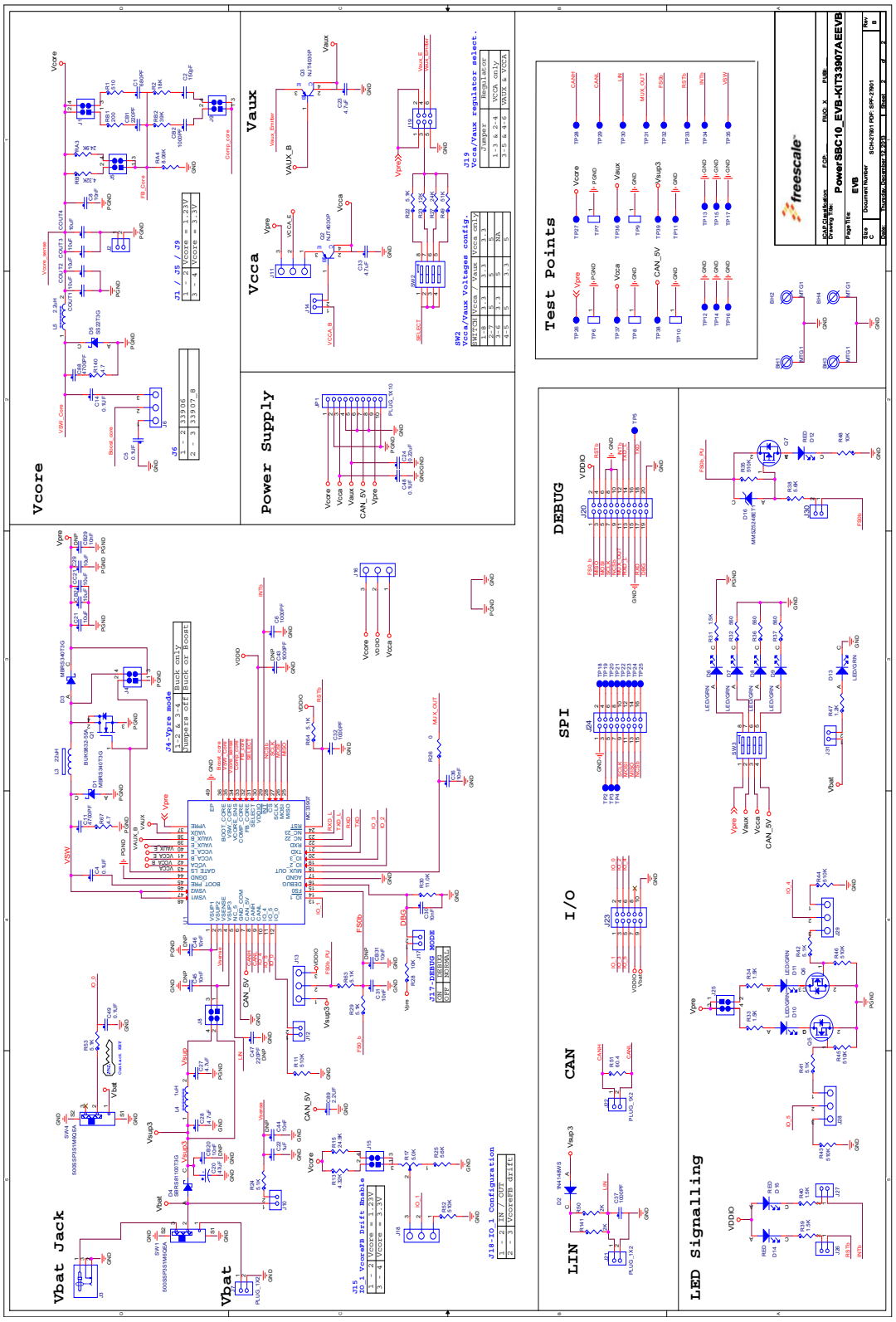
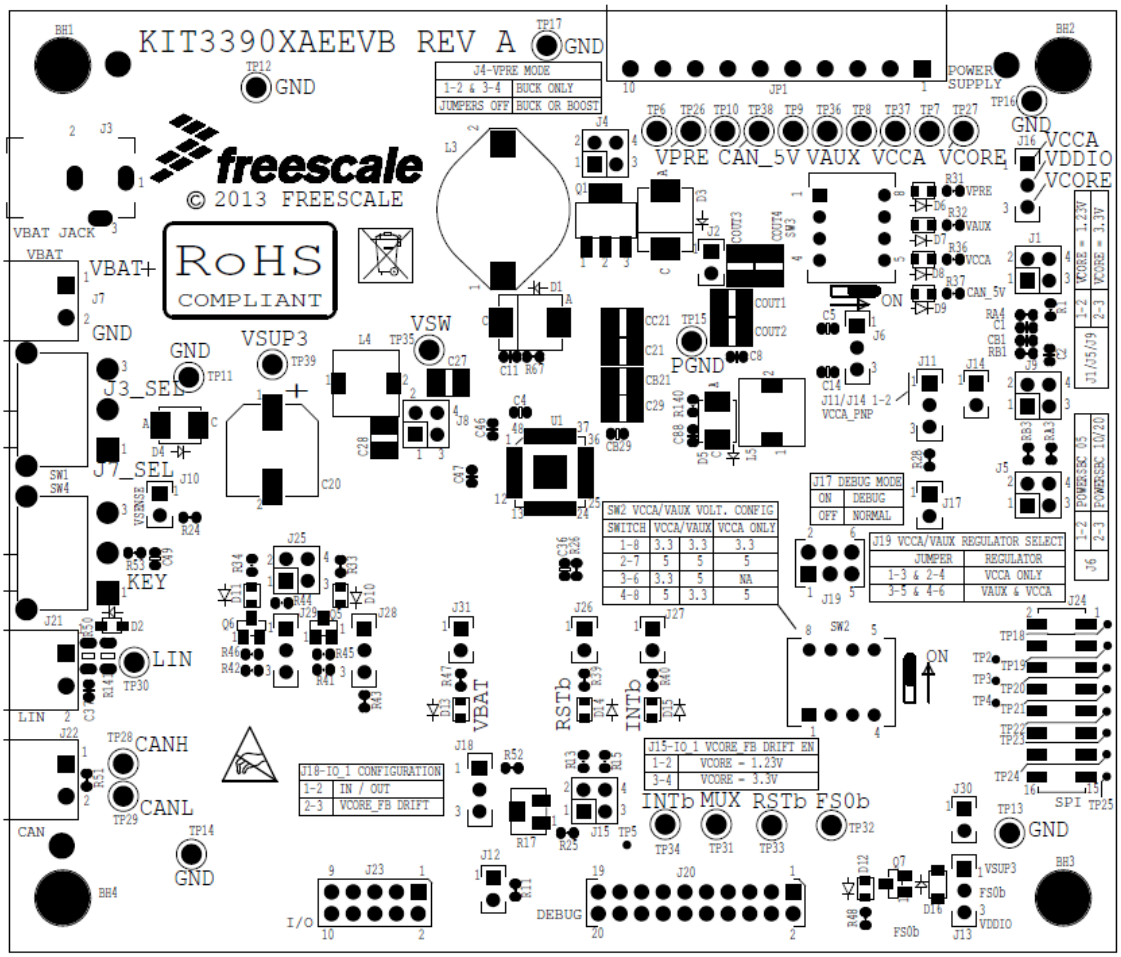


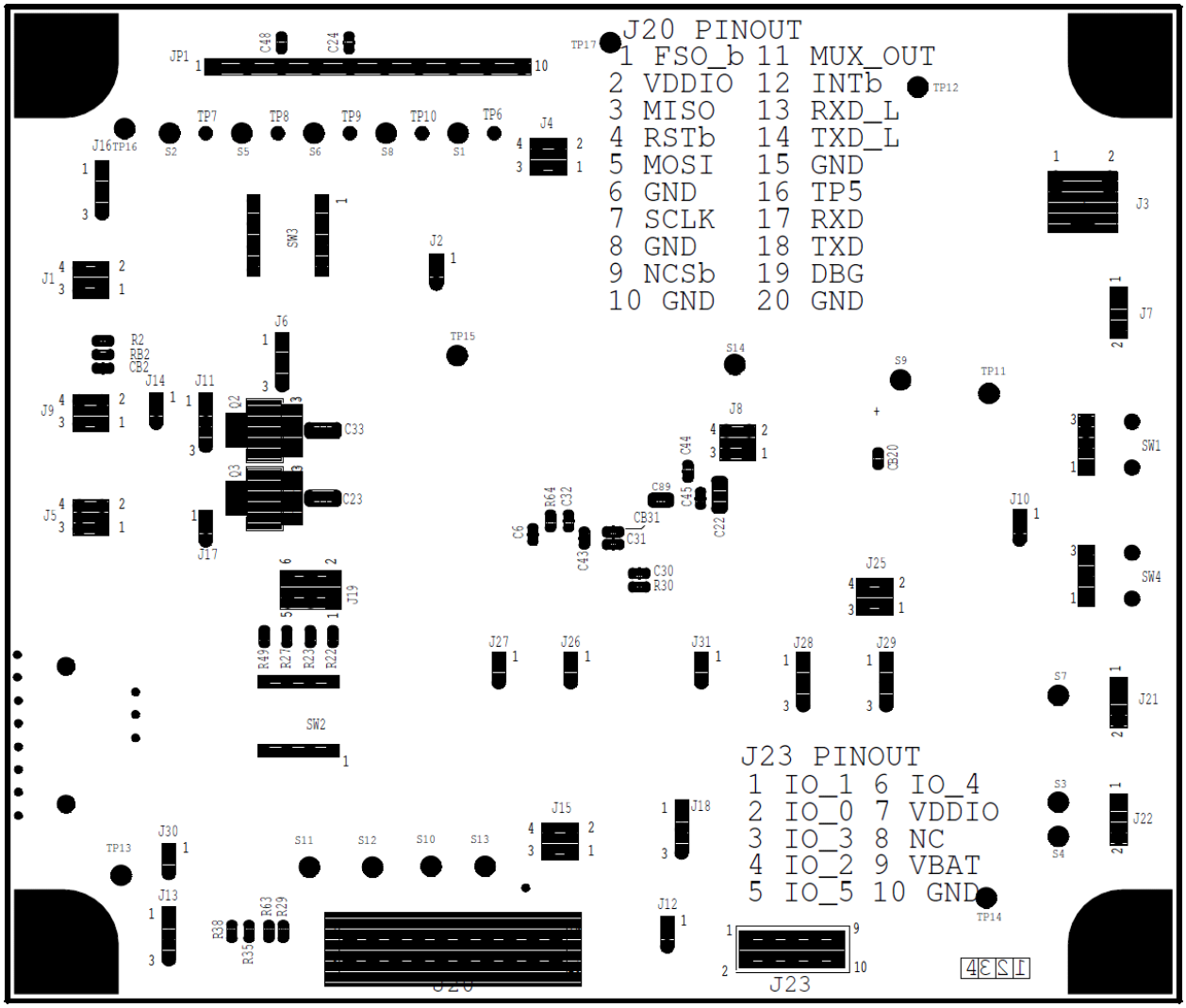
Figure 13. Evaluation Board Schematic

15 Board Layout

15.1 Assembly Layer Top

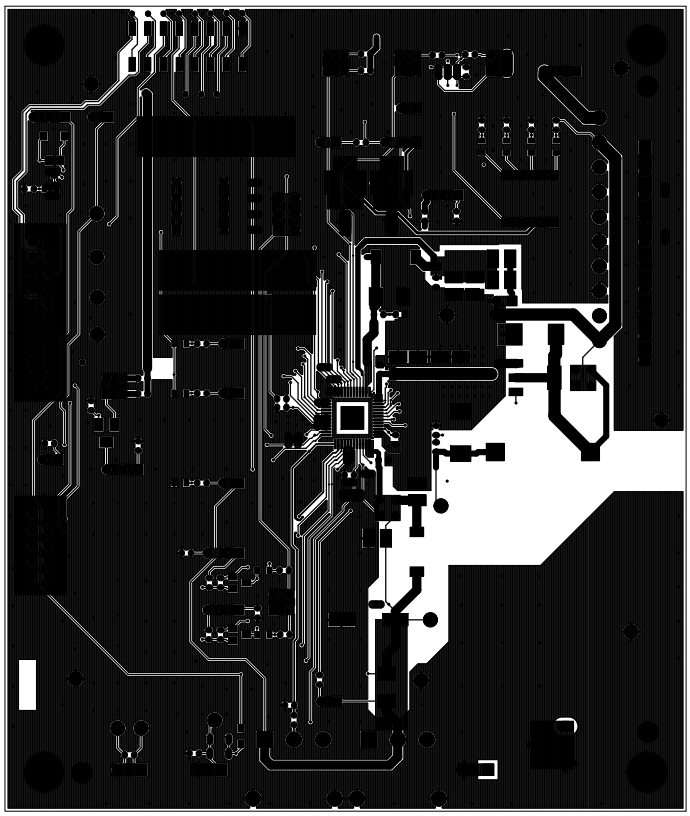


15.2 Assembly Layer Bottom

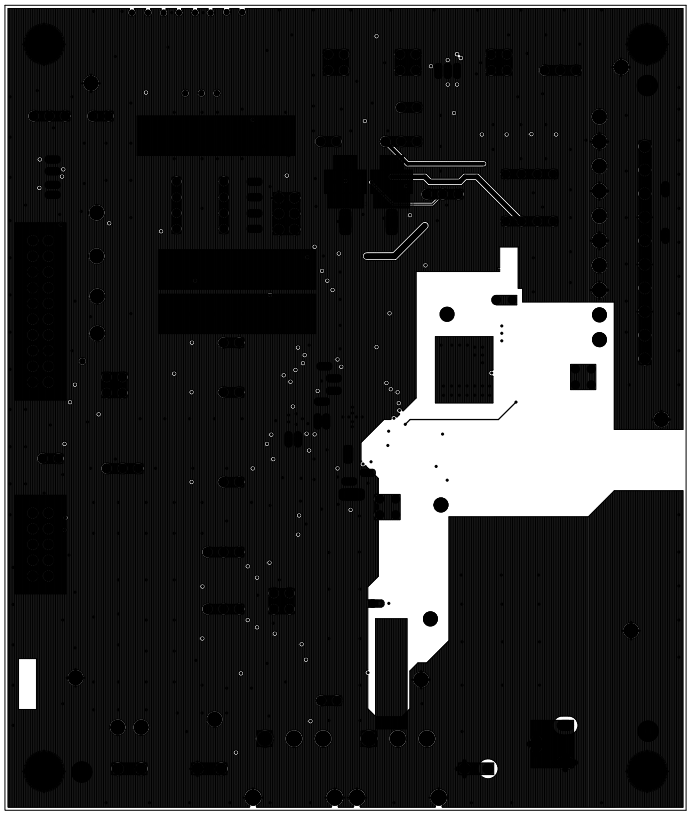


Note: This image is an exception to the standard top-view mode of representation used in this document. It has been flipped to show a bottom view.

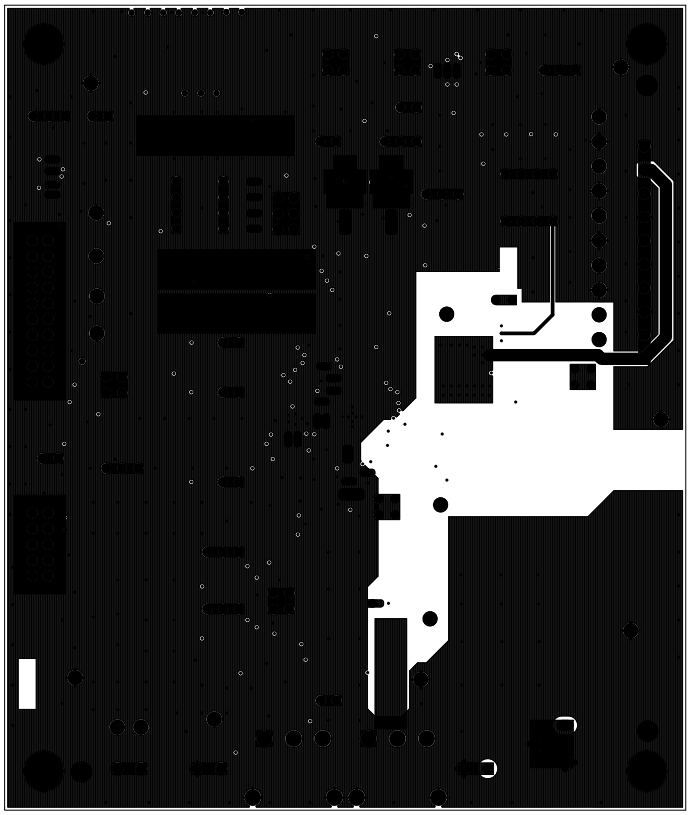
15.3 Top Layer Routing



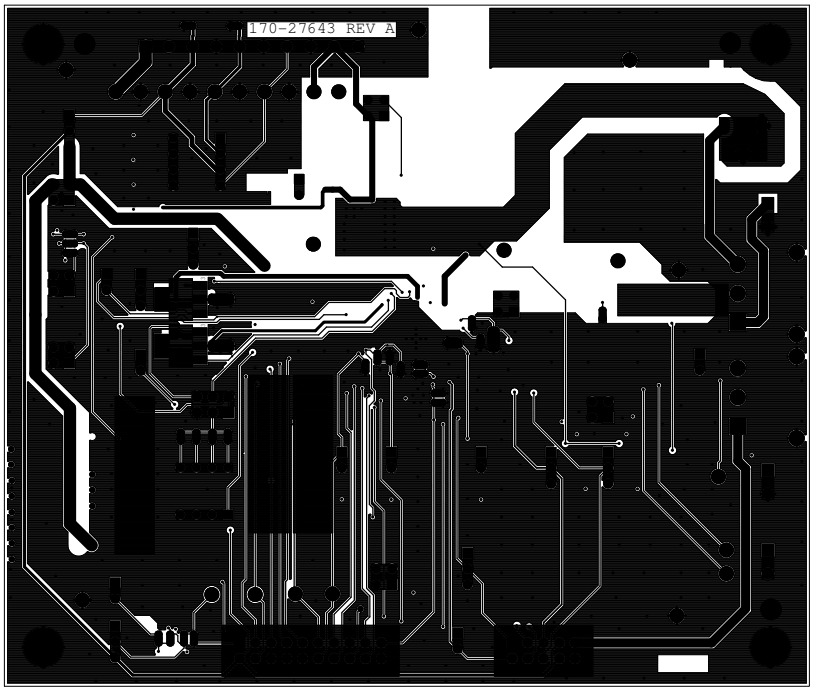
15.4 Inner Layer 1 Routing



15.5 Inner Layer 2 Routing



15.6 Bottom Layer Routing



16 Bill of Material

Table 9. Bill of Materials [1]

Item	Qty	Schematic Label	Value	Manufacturer	Part Number	Assy Opt
1	4	BH1, BH2, BH3, BH4		N/A	MTG1	
2	1	CB1	220 pF	KEMET	C0603C221K5GACTU	
3	4	CB2, C6, C32, C37	1000 pF	AVX	06035U102KAT2A	
4	6	CB20, CB29, CB31, C44, C45, C46	10 nF	AVX	06035C103JAT2A	(2)
5	4	CC21, CB21, C21, C29	10 µF	TDK	CGA6M3X7R1C106K	(3)
6	4	COUT1, COUT2, COUT3, COUT4	10 µF	Murata	GCM32ER71E106KA57	(3)
7	1	C1	680 pF	KEMET	C0603C681J5GAC	
8	1	C2	150 pF	KEMET	C0603C151J5GAC	
9	5	C4, C5, C14, C48, C49	0.1 µF	KEMET	C0603C104K3RAC	
10	4	C8, C30, C31, C36	10 nF	AVX	06035C103JAT2A	
11	2	C11, C88	4700 pF	YAGEO AMERICA	CC0603KRX7R9BB472	
12	1	C20	47 µF	NIPPON CHEMI-CON CORPORATION	EMVH500ADA470MJA0G	
13	1	C22	1.0 µF	TDK	CGA5L3X7R1H105K160AB	
14	2	C23, C33	4.7 µF	Murata	GCM31CR71C475KA37	
15	1	C24	0.22 µF	KEMET	C0603C224K3RACTU	
16	2	C27, C28	4.7 µF	Murata	GCM32ER71H475KA55L	
17	1	C43	1000 pF	AVX	06035U102KAT2A	(2)
18	1	C47	220 pF	KEMET	C0603C221K5GACTU	(2)
19	1	C89	2.2 µF	AVX	08053C225KAT2A	
20	2	D1, D3		ON SEMICONDUCTOR	MBRS340T3G	(3)
21	1	D2		DIODES INC	1N4148WS-7-F	
22	1	D4		ON Semiconductor	SBRS81100T3G	(3)
23	1	D5		ON Semiconductor	SS22T3G	
24	7	D6, D7, D8, D9, D10, D11, D13		OSRAM	LED/GRN LP M67K-E2G1-25	
25	3	D12, D14, D15		OSRAM	RED LS M67K-H2L1-1-0-2-R18-Z	
26	1	D16		ON SEMICONDUCTOR	MMSZ5248BT1G	
27	1	JP1		Phoenix contact	PLUG_1X10 1803358	
28	7	J1, J4, J5, J8, J9, J15, J25		SAMTEC	HDR 2X2 TSW-102-07-G-D	
29	9	J2, J10, J12, J14, J17, J26, J27, J30, J31		SAMTEC	HDR 1X2 TSW-102-07-T-S	
30	1	J3		CUI STACK	CON_1_PWR PJ-102AH	
31	7	J6, J11, J13, J16, J18, J28, J29		TYCO ELECTRONICS	HDR_1X3 826629-3	
32	3	J7, J21, J22		Phoenix contact	PLUG_1X2 1803277	
33	1	J19		TYCO ELECTRONICS	HDR 2X3 1-87215-2	
34	1	J20		SAMTEC	HDR_10X2 TSW-110-07-S-D	
35	1	J23		SAMTEC	HDR 2X5 TSW-105-07-G-D	
36	1	J24		SULLINS ELECTRONICS CORP	NPPC082KFMS-RC	
37	1	L3	22µH	EPCOS	B82479G1223M000	(3)
38	1	L4	1.0 µH	EPCOS	B82472G6102M000	(3)
39	1	L5	2.2 µH	EPCOS	B82472G6222M000	
40	1	Q1		NXP SEMICONDUCTORS	BUK9832-55A,115	(3)
41	2	Q2, Q3		ON Semiconductor	NJT4030PT3G	(3)
42	2	Q5, Q6		ON SEMICONDUCTOR	MMBF0201NLT1G	
43	1	Q7		ON SEMICONDUCTOR	BSS84LT1G	
44	2	RA3, R15	24.9 K	KOA SPEER	RK73H1JTTD2492F	
45	1	RA4	8.06 K	KOA SPEER	RK73H1JTTD8061F	
46	1	RB1	200	KOA SPEER	RK73B1JTTD201J	
47	1	RB2	39 K	KOA SPEER	RK73H1JTTD3902F	
48	2	RB3, R13	4.32 K	KOA SPEER	RK73H1JTTD4321F	
49	1	R1	510	BOURNS	CR0603-JW-511ELF	
50	1	R2	18 K	KOA SPEER	RK73H1JTTD1802F	

Table 9. Bill of Materials [1] (continued)

Item	Qty	Schematic Label	Value	Manufacturer	Part Number	Assy Opt
51	7	R11, R35, R43, R44, R45, R46, R52	510 K	YAGEO AMERICA	RC0603JR-07510KL	
52	1	R17	1.0 K	BOURNS	3224W-1-102E	
53	1	R22	5.1 K	KOA SPEER	RK73H1JTTD5101F	
54	1	R23	12 K	BOURNS	CR0603-JW-123ELF	
55	7	R24, R29, R41, R42, R53, R63, R64	5.1 K	VISHAY INTERTECHNOLOGY	CRCW06035K10JNEA	
56	1	R25	7.15 K	KOA SPEER	RK73H1JTTD7151F	
57	1	R26	0	VISHAY INTERTECHNOLOGY	CRCW06030000Z0EA	
58	1	R27	24 K	PANASONIC	ERJ-3GEYJ243V	
59	2	R28, R48	10 K	KOA SPEER	RK73B1JTTD103J	
60	1	R30	11.0 K	KOA SPEER	RK73H1JTTD1102F	
61	5	R31, R33, R34, R39, R40	1.5 K	BOURNS	CR0603-JW-152ELF	
62	3	R32, R36, R37	560	KOA SPEER	RK73B1JTTD561J	
63	1	R38	5.6 K	KOA SPEER	RK73B1JTTD562J	
64	1	R47	1.2 K	KOA SPEER	RK73H1JTTD1201F	
65	1	R49	51 K	VISHAY INTERTECHNOLOGY	CRCW060351K0JNEA	
66	2	R50, R141	2.0 K	Yageo	RC1206JR-072KL	
67	1	R51	60.4	KOA SPEER	RK73H1JTTD60R4F	
68	2	R67, R140	4.7	BOURNS	CR0603-JW-4R7ELF	
69	2	SW1, SW4		E Switch	500SSP3S1M6QEA	
70	2	SW2, SW3		GRAYHILL	SW_DIP-4_SM 78RB04ST	
71	12	TP2, TP3, TP4, TP5, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25		NOTACOMPONENT	TP_PTH	
72	5	TP6, TP7, TP8, TP9, TP10		Keystone Electronics	5006	[2]
73	7	TP11, TP12, TP13, TP14, TP15, TP16, TP17		KEYSTONE ELECTRONICS	5011 TESTLOOP_BLACK	
74	14	TP26, TP27, TP28, TP29, TP30, TP31, TP32, TP33, TP34, TP35, TP36, TP37, TP38, TP39		KEYSTONE ELECTRONICS	5010 TESTLOOP_RED	
75	1	U1		FREESCALE SEMICONDUCTOR	MC33907AE or MC33908AE	[3]

Notes

1. Freescale does not assume liability, endorse, or warrant components from external manufacturers that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
2. Do not populate
3. **Critical components.** For critical components, it is vital to use the manufacturer listed.

17 References

Following are URLs where you can obtain information on related Freescale products and application solutions:

Freescale.com Support Pages	URL
MC33907 Product Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC33907
KIT33907AEEVB Tool Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KIT33907AEEVB
MC33908 Product Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=MC33908
KIT33908AEEVB Tool Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KIT33908AEEVB
SPIGen Tool Summary Page	http://www.freescale.com/files/soft_dev_tools/software/device_drivers/SPIGen.html
KITUSBSPIDGLEVME Tool Summary Page	http://www.freescale.com/webapp/sps/site/prod_summary.jsp?code=KITUSBSPIDGLEVME
Analog Home Page	http://www.freescale.com/analog
Automotive Home Page	http://www.freescale.com/automotive

17.1 Support

Visit www.freescale.com/support for a list of phone numbers within your region.

17.2 Warranty

Visit www.freescale.com/warranty for a list of phone numbers within your region.

18 Revision History

Revision	Date	Description of Changes
1.0	2/2014	• Initial Release
2.0	3/2014	• Corrected error in Figure 3

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