BLC8G27LS-245AV

Power LDMOS transistor

AMPLEON

Rev. 3 — 2 December 2016

Product data sheet

1. Product profile

1.1 General description

240 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 2500 MHz to 2700 MHz.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C in an asymmetrical Doherty demo board. V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V, unless otherwise specified.

Test signal	f	V _{DS}	P _{L(AV)}	G _p	η_D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2500 to 2690	28	56	14.5	43	-35 [1]

^[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01% probability on CCDF per carrier.

1.2 Features and benefits

- Excellent ruggedness
- High-efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (2500 MHz to 2700 MHz)
- Asymmetric design to achieve optimum efficiency across the band
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

 RF power amplifiers for base stations and multi carrier applications in the 2500 MHz to 2700 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)	0 0 4 0	
2	drain1 (main)	6 2 1 9	2 6
3	gate1 (main)	5	7-1-1
4	gate2 (peak)		3—
5	source	7 3 4 8	4—1—5
6	video decoupling (main)		8 - -
7	n.c.		9
8	n.c.		1
9	video decoupling (peak)		aaa-009150

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	je	
	Name	Description	Version
BLC8G27LS-245AV	_	air cavity plastic earless flanged package; 8 leads	SOT1251-2

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{DS}	drain-source voltage		-	65	V
V _{GS(amp)main}	main amplifier gate-source voltage		-0.5	+13	V
V _{GS(amp)peak}	peak amplifier gate-source voltage		-0.5	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	<u>[1]</u>	-	225	°C

Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}		T_{case} = 80 °C; P_{L} = 56 W; V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V	0.3	K/W

Characteristics 6.

Table 6. **DC** characteristics

 $T_i = 25 \, ^{\circ}$ C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Main dev	rice					
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 1.8 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 180 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V_{DS} = 28 V; I_{D} = 540 mA	1.6	2.1	2.4	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	2.8	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	30	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	280	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 180 mA	-	1.63	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 6.3 \text{ A}$	-	83	135	mΩ
Peak dev	rice			,	1	
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 2.2 \text{ mA}$	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V_{DS} = 10 V; I_{D} = 220 mA	1.5	1.9	2.3	V
V_{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 660 mA	1.6	2.1	2.4	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	2.8	μΑ
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	40	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	280	nA
9 _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 220 mA	-	1.94	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 7.7 \text{ A}$	-	68	112	mΩ

Table 7. **RF** characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; f_1 = 2500 MHz; f_2 = 2690 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit in 2500 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _{L(AV)} = 56 W	12.8	14	-	dB
RLin	input return loss	P _{L(AV)} = 56 W	-	-10	-6	dB
η_{D}	drain efficiency	P _{L(AV)} = 56 W	32	37	-	%
ACPR	adjacent channel power ratio	P _{L(AV)} = 56 W	-	-25	-20	dBc

Test information 7.

7.1 Ruggedness in class-AB operation

The BLC8G27LS-245AV is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V; P_L = 200 W; f = 2500 MHz.

BLC8G27LS-245AV

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7.2 Impedance information

Table 8. Typical impedance of main device

Measured load-pull data of main device; I_{Dq} = 1000 mA; V_{DS} = 28 V. Typical values unless otherwise specified.

f	Z _S [1]	Z _L [1]	P _L [2]	η _D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum pov	wer load				
2500	2.7 – j4.1	1.0 – j4.5	197	56.3	13.1
2600	2.7 – j5.2	1.0 – j4.5	196	56.3	14.1
2700	2.9 – j4.3	1.0 – j4.5	186	54.3	15.7
Maximum dra	in efficiency load				
2500	2.7 – j4.1	1.7 – j3.9	159	62.6	15.2
2600	2.7 – j5.2	1.5 – j3.7	144	61.2	16.5
2700	2.9 – j4.3	1.4 – j4.1	149	58.5	17.2

^[1] Z_S and Z_L defined in Figure 1.

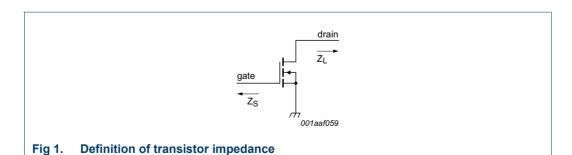
Table 9. Typical impedance of peak device

Measured load-pull data of peak device; I_{Dq} = 1230 mA; V_{DS} = 28 V. Typical values unless otherwise specified.

f	Z _S [1]	Z _L [1]	P _L [2]	η _D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum pov	wer load				
2500	2.5 – j5.6	2.1 – j4.9	256	53.3	13.7
2600	3.9 – j5.1	2.1 – j4.9	254	53.8	14.4
2700	3.4 – j4.2	2.6 – j5.1	240	53.3	15.9
Maximum dra	in efficiency load				
2500	2.5 – j5.6	2.0 – j2.9	187	62.1	16.0
2600	3.9 – j5.1	1.8 – j3.1	177	60.4	16.9
2700	3.4 – j4.2	1.8 – j3.5	174	59.5	18.1

^[1] Z_S and Z_L defined in Figure 1.

^[2] at 3 dB gain compression.



^[2] at 3 dB gain compression.

7.3 VBW in Doherty operation

The BLC8G27LS-245AV shows 110 MHz (typical) video band-width in Doherty demo board in 2600 MHz at V_{DS} = 28 V; I_{Dq} = 500 mA and $V_{GS(amp)peak}$ = 0.5 V.

7.4 Test circuit

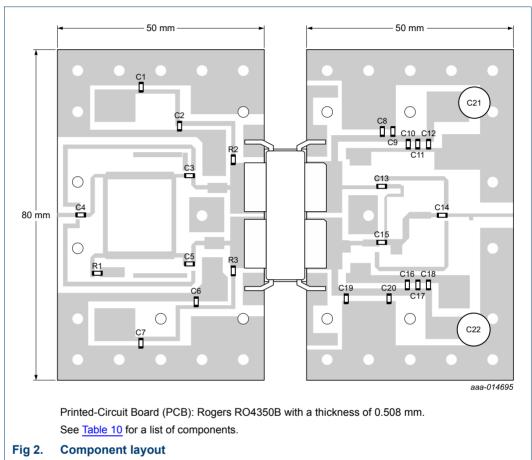
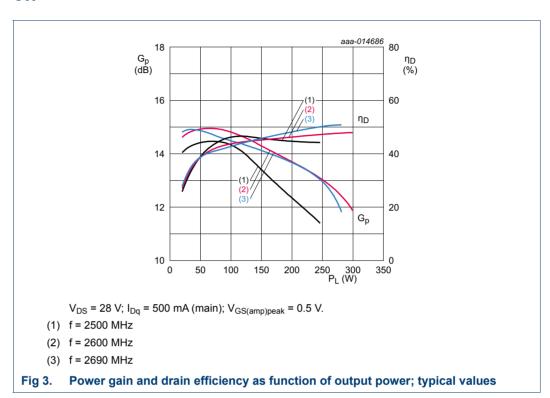


Table 10. List of components For test circuit see Figure 2.

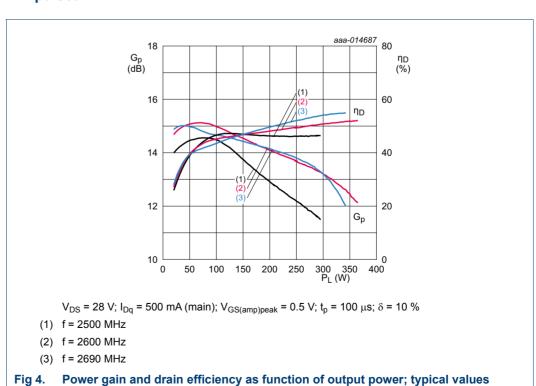
Component	Description	Value	Remarks
C1, C7	multilayer ceramic chip capacitor	0.1 μF, 50 V	Murata
C2, C3, C4, C5, C6, C8, C9, C13, C14, C15, C19, C20	multilayer ceramic chip capacitor	22 pF	ATC 600A
C10, C11, C12, C16, C17, C18	multilayer ceramic chip capacitor	4.7 μF, 50 V	Murata
C21, C22	electrolytic capacitor	2200 μF, 63 V	
R1	resistor	50 Ω	
R2, R3	chip resistor	9.1 Ω	SMD 0805

7.5 Graphical data

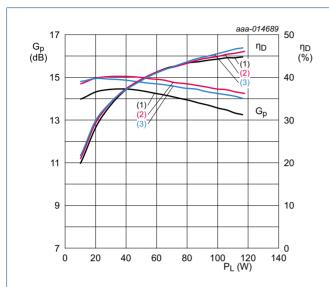
7.5.1 CW



7.5.2 CW pulsed



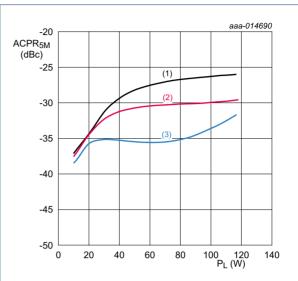
7.5.3 1-Carrier W-CDMA



 V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V.

- (1) f = 2500 MHz
- (2) f = 2600 MHz
- (3) f = 2690 MHz

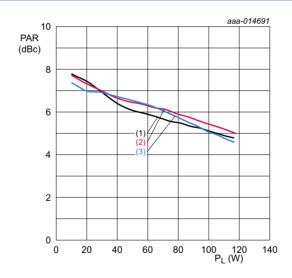
Fig 5. Power gain and drain efficiency as function of output power; typical values



 V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V.

- (1) f = 2500 MHz
- (2) f = 2600 MHz
- (3) f = 2690 MHz

Fig 6. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

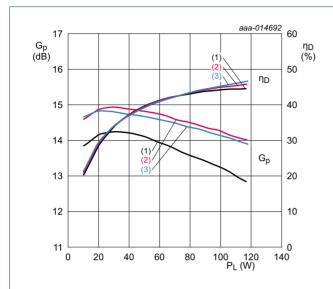


 V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V.

- (1) f = 2500 MHz
- (2) f = 2600 MHz
- (3) f = 2690 MHz

Fig 7. Peak-to-average ratio as a function of output power; typical values

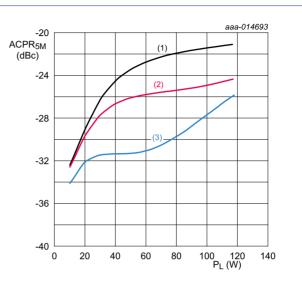
7.5.4 2-Carrier W-CDMA



 V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V.

- (1) f = 2500 MHz
- (2) f = 2600 MHz
- (3) f = 2690 MHz

Fig 8. Power gain and drain efficiency as function of output power; typical values

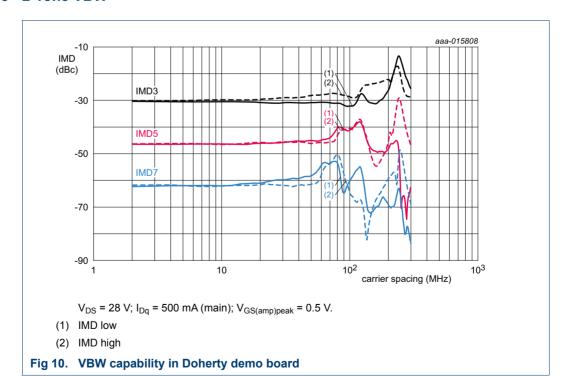


 V_{DS} = 28 V; I_{Dq} = 500 mA (main); $V_{GS(amp)peak}$ = 0.5 V.

- (1) f = 2500 MHz
- (2) f = 2600 MHz
- (3) f = 2690 MHz

Fig 9. Adjacent channel power ratio (5 MHz) as a function of output power; typical values

7.5.5 2-Tone VBW



8. Package outline

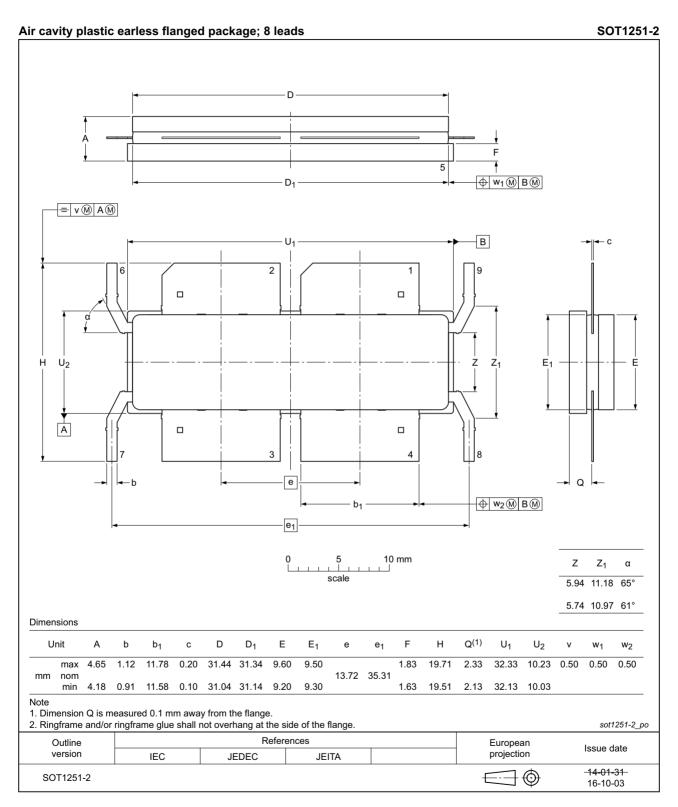


Fig 11. Package outline SOT1251-2

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

- [1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.
- [2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLC8G27LS-245AV v.3	20161202	Product data sheet	-	BLC8G27LS-245AV v.2	
Modifications:	Figure 11 on page 9: updated package outline drawing SOT1251-2				
	Section 9 on page 10: updated Handling information				
BLC8G27LS-245AV v.2	20150901	Product data sheet	-	BLC8G27LS-245AV v.1	
BLC8G27LS-245AV v.1	20141216	Product data sheet	-	-	

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12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions"
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Power LDMOS transistor

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